Listing of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, the method comprising:

storing a full table of line pointers for different sequences of video data to be displayed in the memory; and

operating the driving circuit ~~alternately~~ in ~~a first~~ an address sequence mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder, and in a table update ~~second~~ mode wherein a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means, wherein operating the driving circuit in the table update ~~second~~ mode includes:

setting a base address of the block of line pointers to zero;

reading a line pointer that corresponds to the base address of zero from the memory into the address table register means; and

successively increasing the base address by one and reading the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means.

2. (Currently Amended) Driving circuit for a display system comprising:

a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers;

means for successively updating the address table register means with subsequent blocks of line pointers from the full table of line pointers that is contained in the memory, ~~,~~ wherein the means for successively updating the address table register means with the subsequent blocks of line pointers is configured to set a base address of a block of line pointers to zero, to read a line pointer that corresponds to the base address of zero from the memory into the address table register means, to successively increase the base address by one and to read the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means;

a pixel counter, the output of which in combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder determines the addresses for said video data; and

switching means, by which ~~alternately~~ memory addresses for video data are generated in ~~a first~~ an address sequence mode in the address sequencer, and in a table update ~~second~~ mode the address table register is updated with a next block of line pointers from the full table of line pointers that is contained in the memory.

3. (canceled)

4. (Previously Presented) Driving circuit as claimed in claim 2, characterized in that the memory comprises a full table of line pointers for different sequences of video data to be displayed.

5. (previously presented) Apparatus for displaying images comprising a display system and a driving circuit according to claim 2.

6. (canceled)

7. (Previously Prepared) The driving circuit of claim 2 further comprising a computer readable medium that stores a computer readable program embedded therein, said computer readable program capable of running on a signal processor in the driving circuit.

8. (canceled)

9. (Currently Amended) Driving circuit for a display system comprising:

a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers for different sequences of video data to be displayed, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers;

means for successively updating the address table register means with subsequent blocks of line pointers from the full table of line pointers that is contained in the memory, ~~,~~ wherein the means for successively updating the address table register means with the subsequent blocks of line pointers is configured to set a base address of a block of line pointers to zero, to read a line pointer that corresponds to the base address of zero from the memory into the address table register means, to successively increase the base address by one and to read the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means; and

a pixel counter, the output of which in combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder determines the addresses for said video data.

10. (previously presented) The driving circuit of claim 5 further comprising a computer readable storage medium that stores a computer program that runs on a signal processing means in the driving circuit.

11. (Currently Amended) The method of claim 1, wherein operating the driving circuit in the address sequence ~~first~~ mode includes:

setting the line counter to zero;

generating consecutive pixel addresses for video data that corresponds to the line counter of zero; and

successively increasing the line counter by one and generating corresponding pixel addresses until the last line pointer of the block of line pointers is read out.

12. (Previously Presented) Driving circuit as claimed in claim 2, wherein the line counter is set to zero, consecutive pixel addresses for video data that corresponds to the line counter of zero are generated, and the line counter is successively increased by one and corresponding pixel addresses are generated until the last line pointer of the block of line pointers is read out.

13. (Previously Presented) Driving circuit as claimed in claim 9, wherein the line counter is set to zero, consecutive pixel addresses for video data that corresponds to the line counter of zero are generated, and the line counter is successively increased by one and corresponding pixel addresses are generated until the last line pointer of the block of line pointers is read out.

14. (Currently Amended) The method of claim 1, wherein operating the driving circuit in the address sequence ~~first~~ mode includes:

setting the line counter to zero;

generating consecutive pixel addresses for video data that corresponds to the line counter of zero;

transferring the video data with the generated consecutive pixel addresses to the display; and

successively increasing the line counter by one, generating corresponding pixel addresses, and transferring video data with the generated corresponding pixel addresses to the display until the last line pointer of the block of line pointers is read out.

15. (Previously Presented) Driving circuit as claimed in claim 2, the line counter is set to zero, consecutive pixel addresses for video data that corresponds to the line counter of zero are generated, the video data with the generated consecutive pixel addresses is transferred to the display, the line counter is successively increased by one, corresponding pixel addresses are

generated, and video data with the generated corresponding pixel addresses is transferred to the display until the last line pointer of the block of line pointers is read out.

16. (Previously Presented) The method of claim 1 further comprising moving the block of line pointers in the address table register means into the memory.

17. (Previously Presented) Driving circuit as claimed in claim 9, wherein a block of line pointers in the address table register means is moved into the memory.

18. (Previously Presented) Driving circuit as claimed in claim 2, wherein a block of line pointers in the address table register means is moved into the memory.

19. (Previously Presented) The method of claim 16 further comprising:

downloading a first block of line pointers from the memory into the address table register means;

transferring video data that corresponds to the first block of the line pointers to the display; and

successively downloading next blocks of line pointers from the memory into the address table register means and transferring corresponding video data to the display until the last block of line pointers of the full table stored in the memory is downloaded from the memory into the address table register means.

20. (Previously Presented) Driving circuit as claimed in claim 17, a first block of line pointers is downloaded from the memory into the address table register means, video data that corresponds to the first block of the line pointers is transferred to the display, and next blocks of line pointers are successively downloading from the memory into the address table register means and corresponding video data is transferred to the display until the last block of line pointers of the full table contained in the memory is downloaded from the memory into the address table register means.

21. (Previously Presented) Driving circuit as claimed in claim 18, wherein a first block of line pointers is downloaded from the memory into the address table register means, video data that corresponds to the first block of the line pointers is transferred to the display, and next blocks of line pointers are successively downloading from the memory into the address table

register means and corresponding video data is transferred to the display until the last block of line pointers of the full table contained in the memory is downloaded from the memory into the address table register means.